Design Paradigm for Robust Spin Torque Transfer Magnetic RAM (STT MRAM) From Circuit/Architecture Perspective

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Introduction

Principle of MRAM

Change State use magnetic field

High resistance state

Low resistance state

Free Layer

Fixed layer
**STT-MRAM**

**(a) Conventional MRAM Cell**

- 20-30 F²

- Current I

**(b) STT-RAM Cell**

- 6 F²

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*Write Current:*  \( I_{sw} \sim \frac{1}{\text{Volume}} \)

*Characteristic:*  \( I_{sw} \sim \text{Volume} \)
Use 1 transistor
Vgs and Vdd is same when read an write
(-> only transistor size can control current)
Due to they use same amount of current read and write
Only distinguish read and write operation with pulse time width
Decision Failure
These phenomena represent read-failure events caused by the wrong decision made by the sensing circuitry.

Disturbance Failure
A cell flip during read operation
Because read & write current use same path
Write Failure
Ic = Critical current

Relationship

Disturbance Failure
Decision Failure
Write Failure

Iop
Relationship

Disturbance Failure
Decision Failure
Write Failure

$Ic = \text{Critical current}$

$Iop$
Read Failure

Disturb failure probability vs. NMOS width (µm)

- MEM. data prob. = 25%
- MEM. data prob. = 50%
- MEM. data prob. = 75%
Read Failure

![Graph showing decision failure probability vs NMOS width (um) for different memory data probabilities.](image-url)
Write Failure

Write failure probability

NMOS width (μm)

MEM. data prob. = 25%
MEM. data prob. = 50%
MEM. data prob. = 75%
Optimal point
**Proposed Solution**

(a) Proposed Solution Diagram

- Wordline (WL)
- Bitline (BL)
- Source Line (SL)
- $R_{MTJ}$

(b) Read-Wordline (WL_r)
- Write-Wordline (WL_w)
- BL
- SL
- Read-NMOS
- Write-NMOS
Ic = Critical current

Disturbance Failure
Decision Failure
Write Failure
Relaxation – Reliability Issue

Disturbance Failure

$I_c = \text{Critical current}$

$I_{\text{write}}$

$I_{\text{read}}$

Retention Time

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[1] Design Paradigm for Robust Spin Torque Transfer Magnetic RAM (STT MRAM) From Circuit / Architecture Perspective


[3] Failure and reliability analysis of STT-MRAM