Design of Non-destructive Single-sawtooth Pulse Based Readout for STT-RAM by NVM-SPICE

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Due to process variations, decision failure is a severe issue in STT-RAM design

1. Conventional Sensing Scheme
2. Conventional Self-Reference Sensing Scheme
3. Nondestructive Self-reference Sensing Scheme
4. Single-sawtooth pulse based readout
Conventional Sensing Scheme

\[ I \cdot R_L < V_{\text{ref}} < I \cdot R_H \]
Conventional Sensing Scheme

Problem

\[ \text{Max}(R_L + R_{TR}) < \text{Min}(R_H + R_{TR}) \]

This might not be satisfied when all of the memory cells are considered, which consequently results in read failure.
1. Read MTJ and Store C1
2. Write “0”
3. Read “0” current $I_2(>I_1)$

$I_1*(R_{L1}+R_{TR1}) < I_2*(R_{L2}+R_{TR2}) < I*R_{H1}*(R_{TR1})$
\[ \alpha = \frac{I_2}{I_1} \text{ (read current ratio)} \]

\[ \text{Max}\left( \frac{R_{L1}+R_{TR1}}{R_{L2}+R_{TR2}} \right) < \text{Min}\left( \frac{R_{H1}+R_{TR1}}{R_{L2}+R_{TR2}} \right) \]

4. Write Back
Problem

Two write operation

-> long latency period

-> large power consumption
Nondestructive Self-reference Sensing Scheme
Nondestructive Self-reference Sensing Scheme

\[ \alpha = \frac{I_2}{I_1} \]
\[ \beta = \frac{V_3}{V_2} \]

\[ V_1 = I_1(R_{L1} + R_{T1}) < V_3 = \alpha I_2(R_{L2} + R_{T2}) \]
\[ V_3(\alpha I_2(R_{H2} + R_{T2})) < V_1 = \alpha I_1(R_{H1} + R_{T1}) \]
Problem

\[
\max\left(\frac{R_{L1}+R_{TR1}}{R_{L2}+R_{TR2}}\right) < \min\left(\frac{R_{H1}+R_{TR1}}{R_{H2}+R_{TR2}}\right)
\]

To satisfy this equation -> Small margin

Sensing margin is big problem
Single-sawtooth pulse based readout

\[ i(t) = K_s t \]
Single-sawtooth pulse based readout

Rap(i) = RH - Kap * i
Rp(i) = RL - Kp * i

VBL,AP(t) = I(t) * R(i) = RH * Ks * t - Kap * ks^2 * t^2
VBL,P(t) = I(t) * R(i) = RL * Ks * t - Kp * ks^2 * t^2

d2(VBL,AP)/dt^2 = -2 * Kap * Ks^2
d2(VBL,AP)/dt^2 = -2 * Kp * ks^2

Kp is a close to zero
Single-sawtooth pulse based readout

\[ i(t) = K_s t \]
### Conclusion

<table>
<thead>
<tr>
<th>Scheme</th>
<th>Read latency</th>
<th>Sense margin (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>destructive readout [2]</td>
<td>2 read cycles + 2 write cycles</td>
<td>76.6</td>
</tr>
<tr>
<td>non-destructive readout [3]</td>
<td>2 read cycles</td>
<td>12.1</td>
</tr>
<tr>
<td>proposed</td>
<td>1 read cycle</td>
<td>15 (hybrid)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100 (OPAMP)</td>
</tr>
</tbody>
</table>

**Problem**

1. 1 read cycle [propose] > 2 read cycles[3] possible
2. Op- amp Feed-back
3. RC-base high pass filter
Sensing Circuit is really critical for read latency.

If we choose proper sensing circuit, we can improve read latency as well as read accuracy.

[2] A 0.24um 2.0v t1mtj 16-kb nonvolatile magnetoresistance ram with self-reference sensing scheme


[4] Spice macromodel of spin-torque-transfer-operated magnetic tunnel junctions