Multilevel Phase-Change Memory

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Phase Change Memory

Low Latency
High Endurance
Long Retention
High Scalability

<table>
<thead>
<tr>
<th>Attributes</th>
<th>PCM</th>
<th>EEPROM</th>
<th>NOR</th>
<th>NAND</th>
<th>DRAM</th>
</tr>
</thead>
<tbody>
<tr>
<td>Non-Volatile</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Scalability</td>
<td>&lt;10 nm</td>
<td>~4x</td>
<td>~3x nm</td>
<td>~1x nm</td>
<td>~2x nm</td>
</tr>
<tr>
<td>Bit Alterable</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
</tr>
<tr>
<td>Erase Required</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Software</td>
<td>Easy</td>
<td>Easy</td>
<td>Moderate</td>
<td>Hard</td>
<td>Easy</td>
</tr>
<tr>
<td>Write Speed</td>
<td>~100 MB/s</td>
<td>~30 KB/s</td>
<td>~1 MB/s</td>
<td>~20 MB/s</td>
<td>~1 GB/s</td>
</tr>
<tr>
<td>Read Speed</td>
<td>50 - 100 ns</td>
<td>~200 ns</td>
<td>70-100 ns</td>
<td>15-50 µs</td>
<td>20 - 80 ns</td>
</tr>
<tr>
<td>Endurance</td>
<td>$10^6 \diamond 8$</td>
<td>$10^5-6$</td>
<td>$10^5$</td>
<td>$10^4-5$</td>
<td>Unlimited</td>
</tr>
</tbody>
</table>
Amorphous Phase (RESET)
High Resistivity

Poly-crystalline Phase (SET)
Row Resistivity
RESET – High amplitude & Sharp programming pulse – Retain the disorder of the liquid phase
SET – Longer Pulse – Hold for sufficient time to allow crystallization
READ – Small voltage to avoid read disturbance
I-V Characteristic – Read Operation
Multilevel storage in PCM is achieved by accurate programming of the memory cell into intermediate resistance levels between the RESET and SET States.
4 Iterations

Program and Verify
Program and Verify
4 Level Cell
8 Level Cell
Retention Time
Conclusion

Experimental characterization of Multilevel PCM cells

Feasibility of Multilevel programming (Iterative Program and Verify Schemes)

4 Distinct Level – 4~8 Iterative Steps