Optimizing NAND Flash-Based SSDs via Retention Relaxation

Ren-Shuo Liu, Chia-Lin Yang, and Wei Wu
Motivation

NAND Flash is typically required to retain data for 1 to 10 years.

Many data are overwritten in hours or days in several popular workloads in data centers.

The gap between the specification guarantee and actual programs’ needs can be exploited to improve write speed or ECC’s cost and performance.
A chargeable floating gate is introduced to tune the transistor threshold voltage.
Operating Principle

Program
Write (Program) - ISPP

Smaller $\Delta V_p$ -> more precise $V_{th}$

Large $\Delta V_p$ -> Fast Write

Retention Relaxation
Relaxation Retention

(a) ISPP with large $\Delta V_P$

(b) ISPP with small $\Delta V_P$
Relaxation Retention
Relaxation Retention

![Graph showing NAND Flash Write Speedup vs. Data Retention (Year)].

- **Typical case**
- **Corner cases**

<table>
<thead>
<tr>
<th>Retention</th>
<th>Speedup</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 year</td>
<td>1x</td>
</tr>
<tr>
<td>10 weeks</td>
<td>1.86x</td>
</tr>
<tr>
<td>2 weeks</td>
<td>2.33x</td>
</tr>
</tbody>
</table>
The data retention requirement of a sector written
the interval from the time the sector is written to the time the sector is overwritten.
Retention Time Requirement

(a) MSRC workloads

(b) MapReduce and TPC-C workloads
LDPC
Extra Write

The bar chart compares the annual average extra write # between RR-10week and RR-2week for various workloads. The chart shows a significant increase in extra writes for Rd1 and Rd2 compared to the other workloads.
Overall Response Time

Bar chart showing the overall response time speedup for different workloads and different strategies: Baseline, RR-10week, and RR-2week.
They present NAND flash retention relaxation and proposed ECC architecture.

They optimize the write speed and ECC’s cost and performance.