

# Optimizing NAND Flash-Based SSDs via Retention Relaxation

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## Motivation

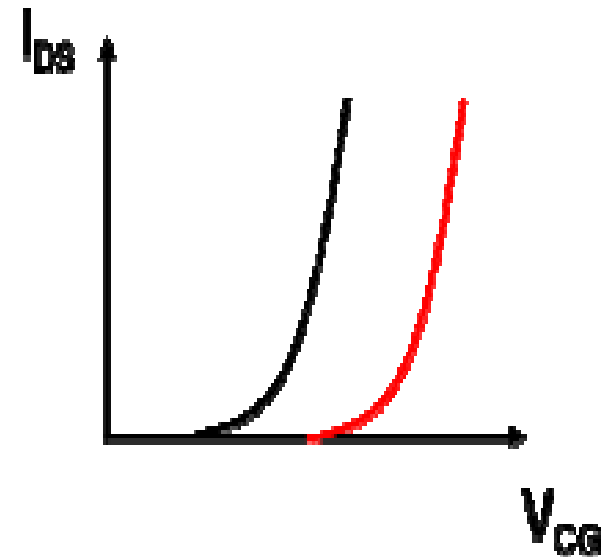
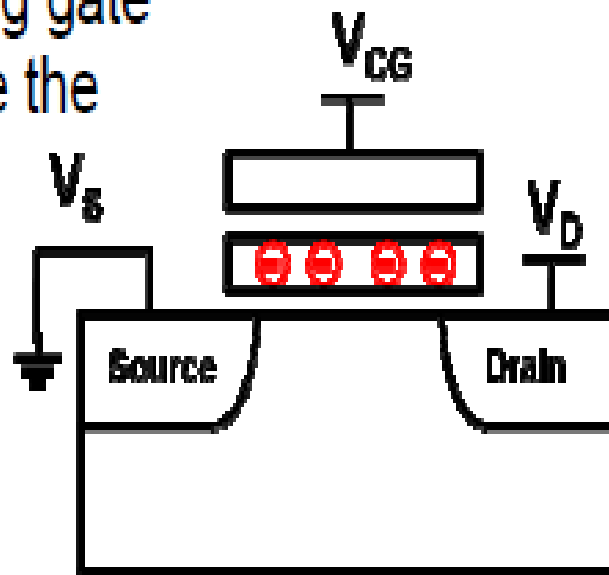
NAND Flash is typically required to retain data for 1 to 10 years

Many data are overwritten in hours or days  
in several popular workloads in data centers

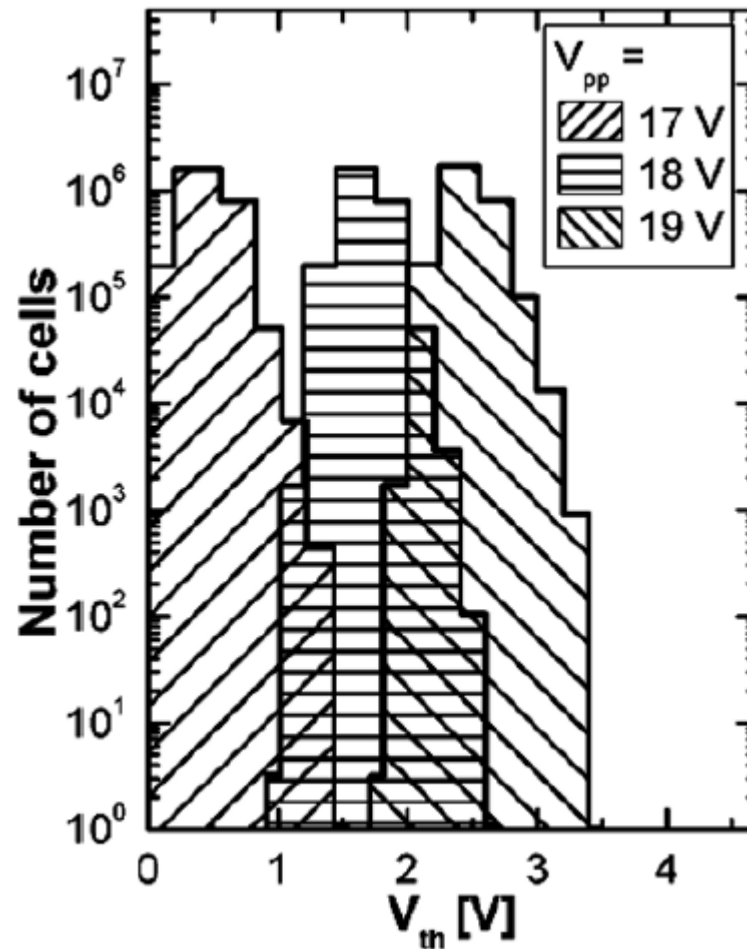
The gap between  
the specification guarantee and actual programs' needs  
can be exploited to improve write speed or ECC's cost and performance

## Memory principle

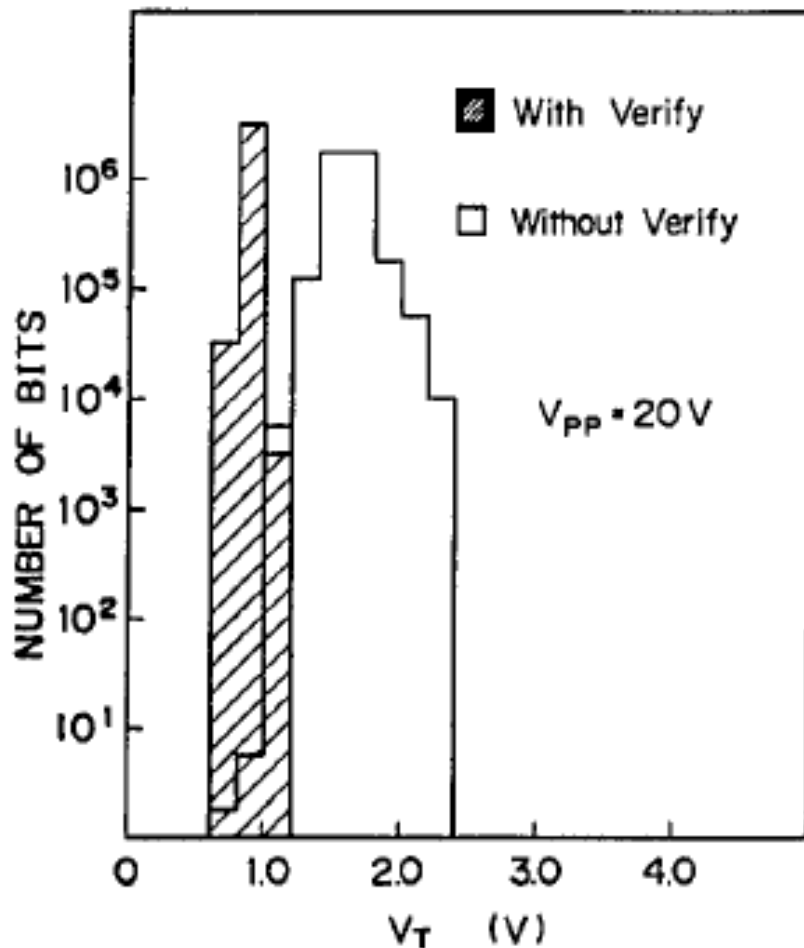
- A chargeable floating gate is introduced to tune the transistor threshold voltage



## Program



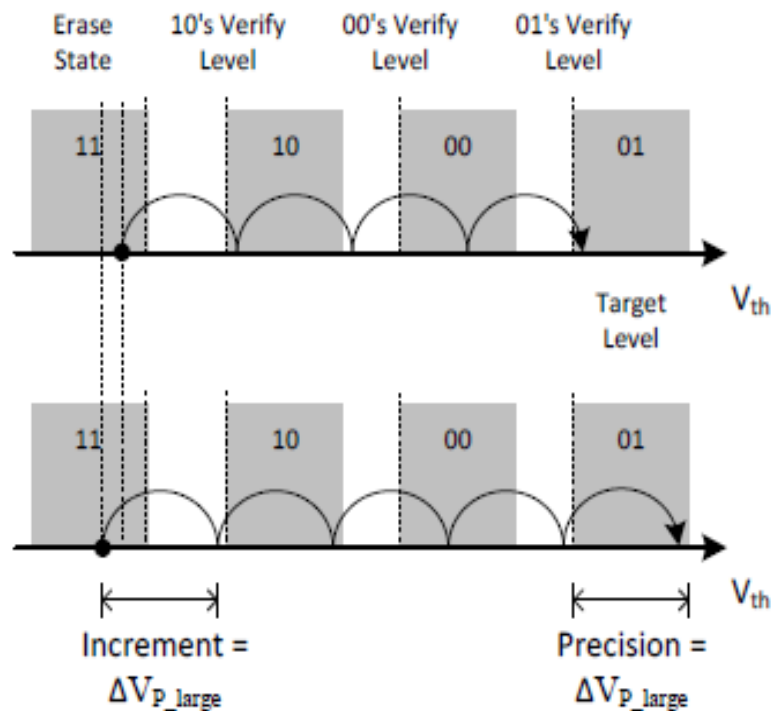
## Write (Program) - ISPP



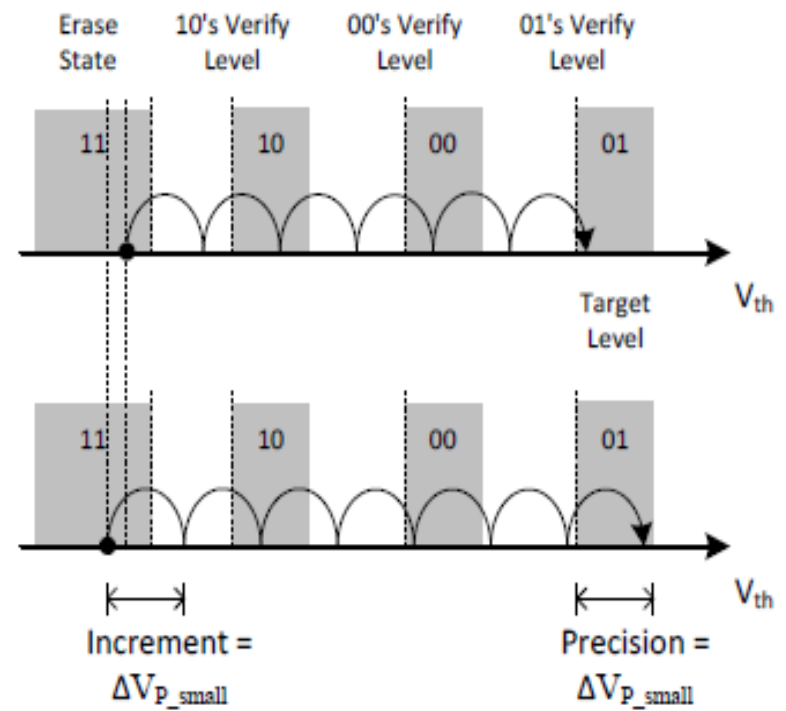
Smaller  $\Delta V_p \rightarrow$  more precise  $V_{th}$

Large  $\Delta V_p \rightarrow$  Fast Write  
Retention Relaxation

## Relaxation Retention

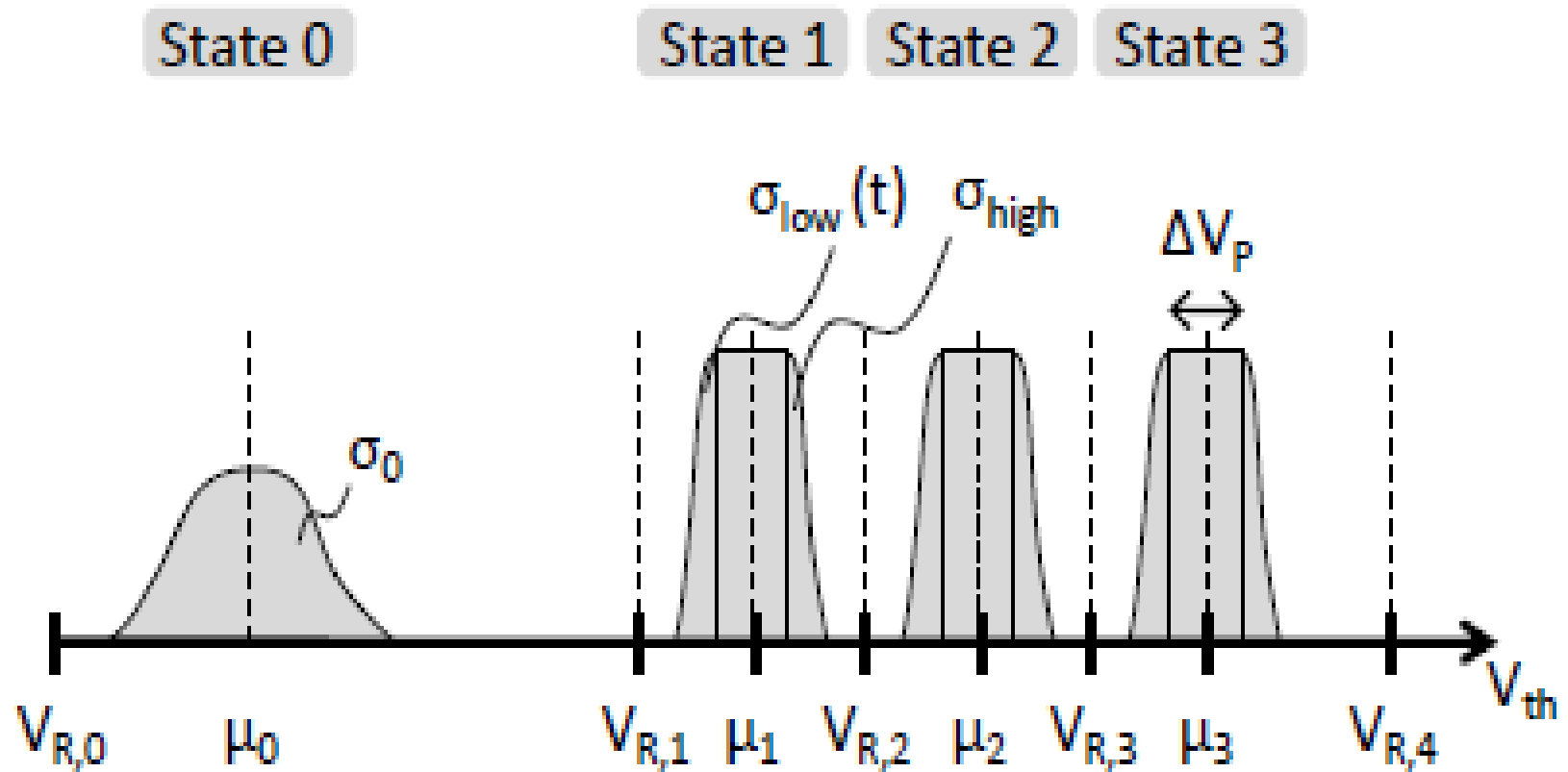


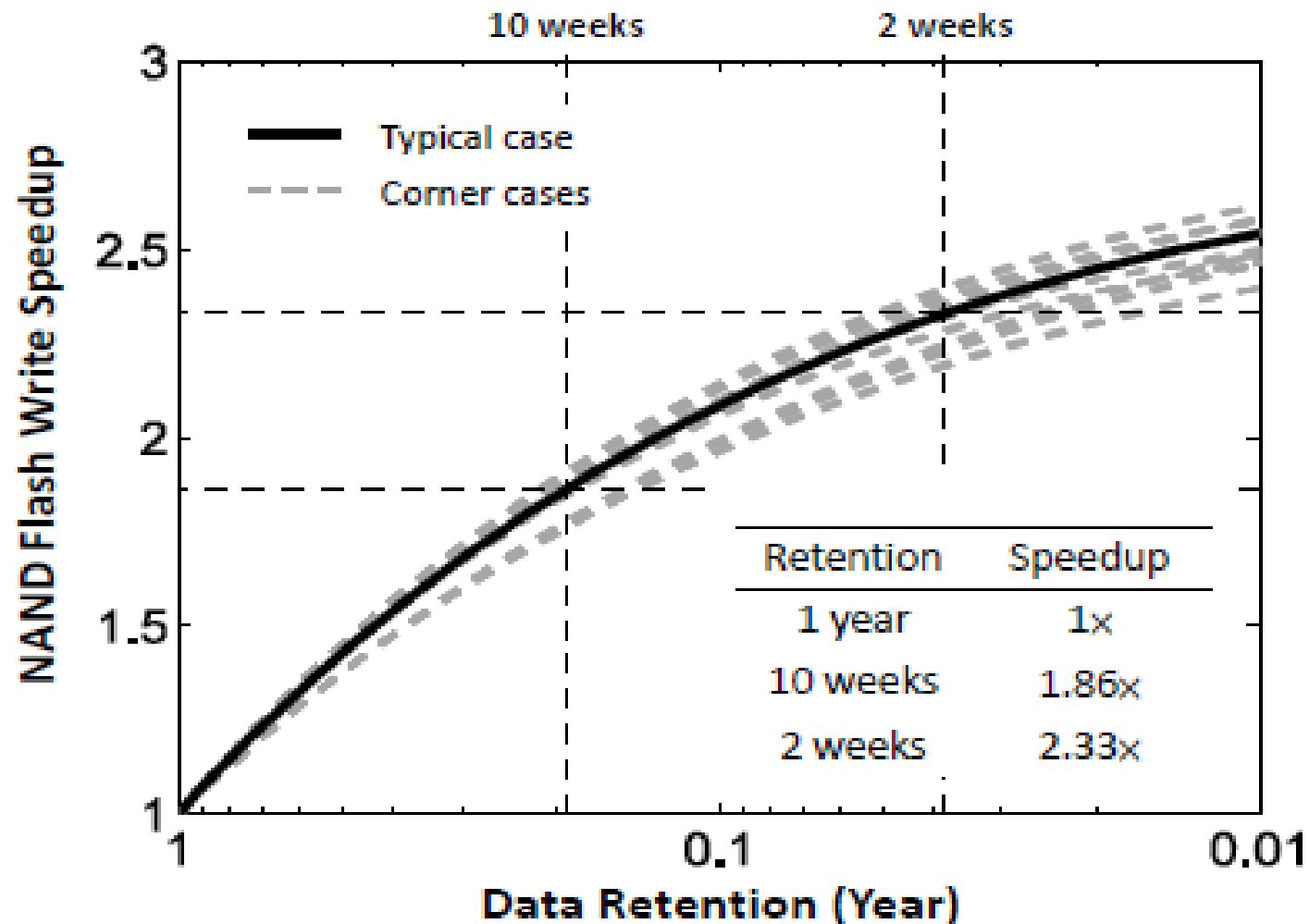
(a) ISPP with large  $\Delta V_p$



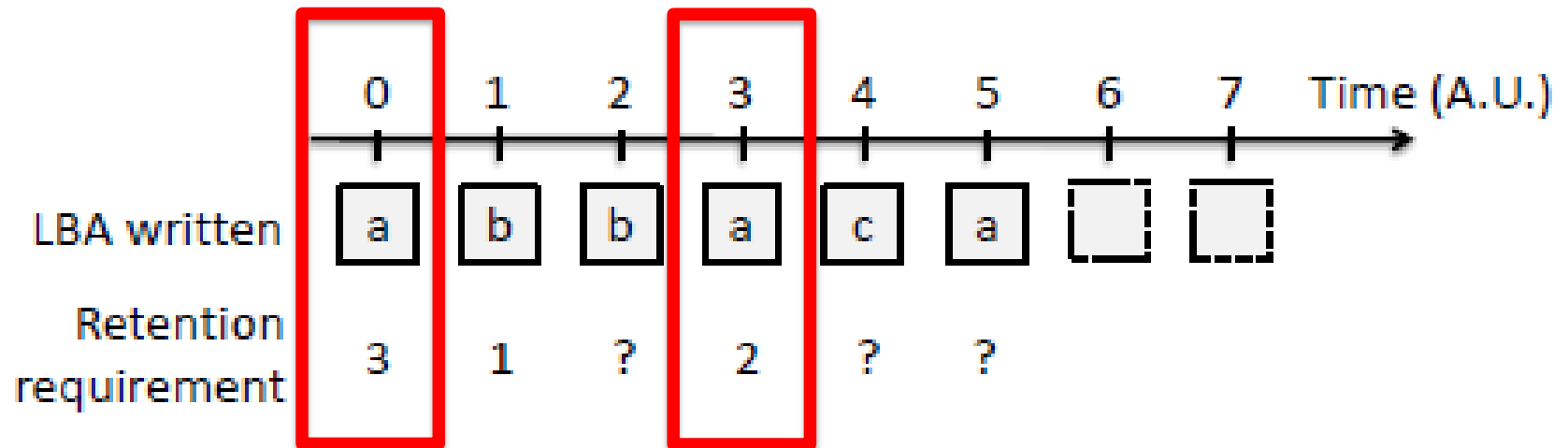
(b) ISPP with small  $\Delta V_p$

## Relaxation Retention



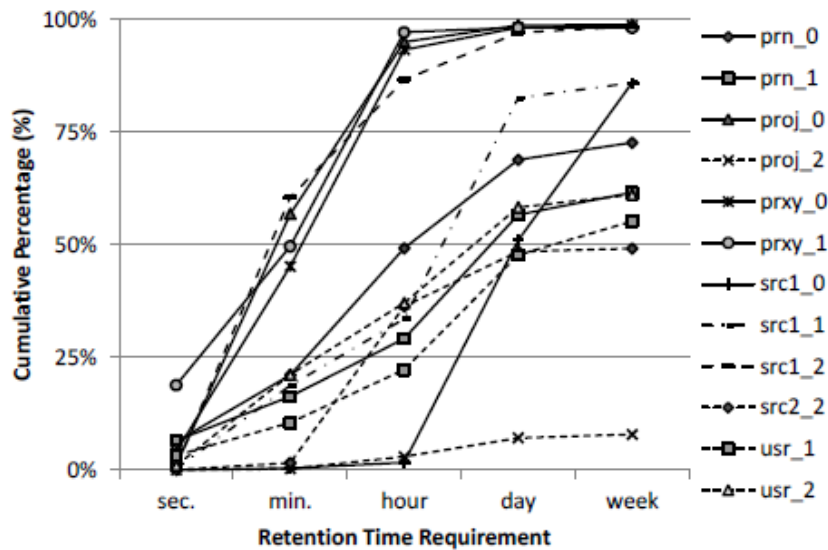


# Retention Time Requirement

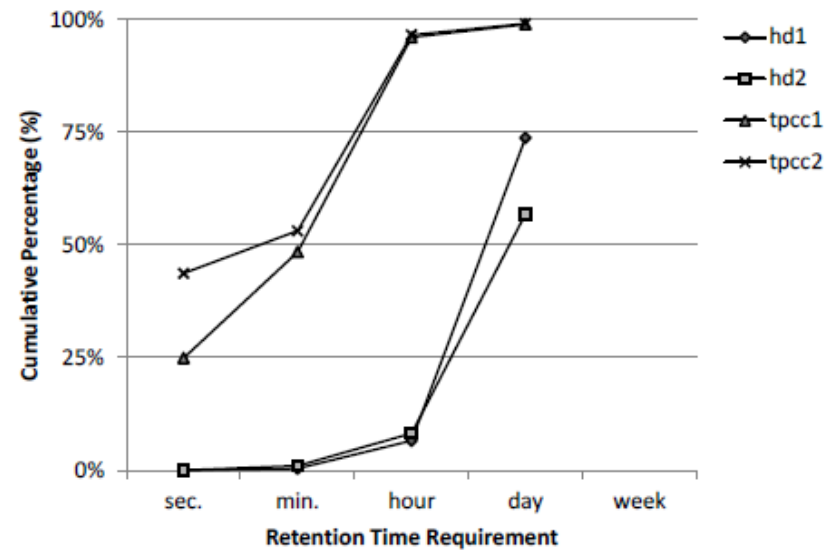


The data retention requirement of a sector written the interval from the time the sector is written to the time the sector is overwritten.

## Retention Time Requirement

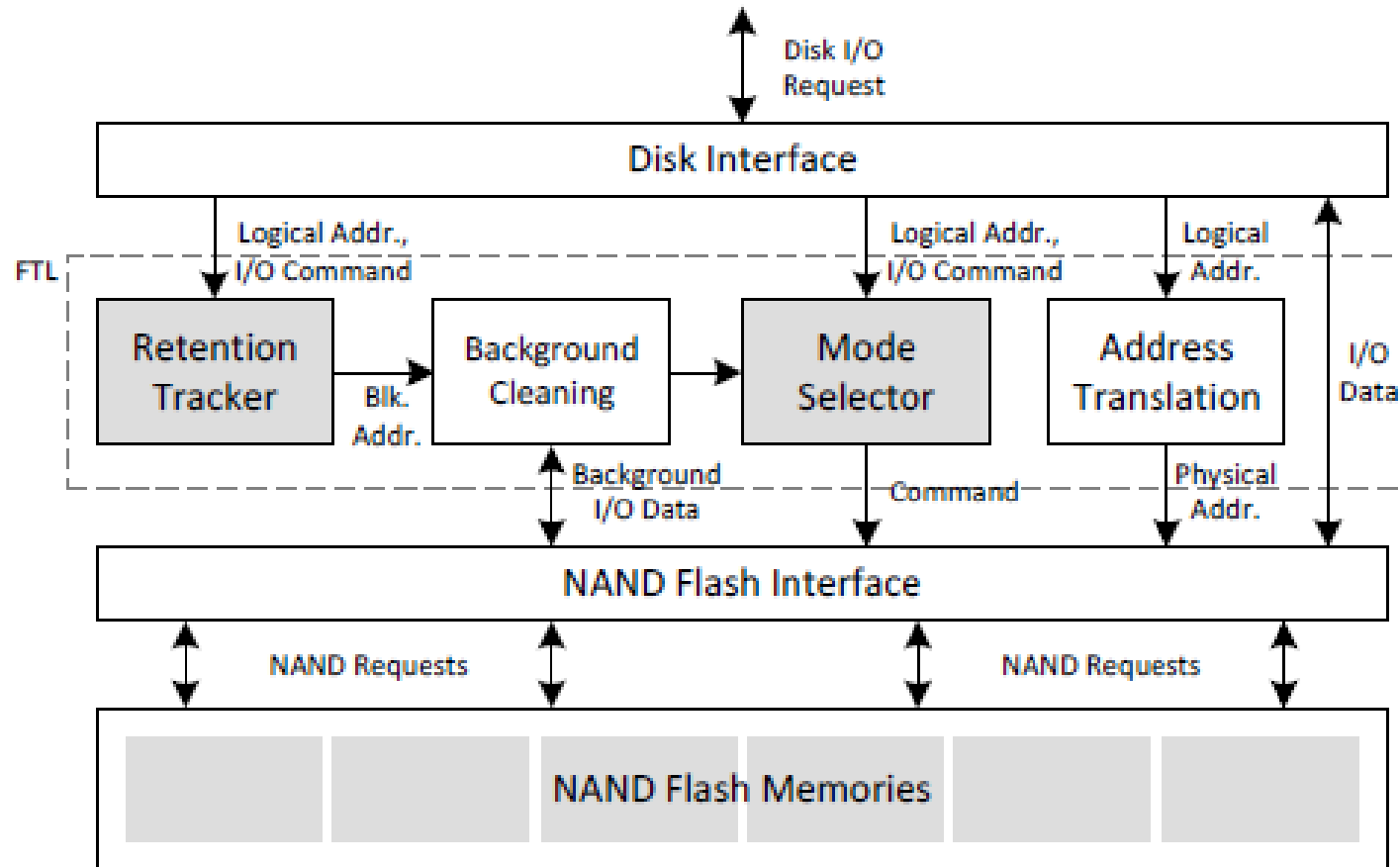


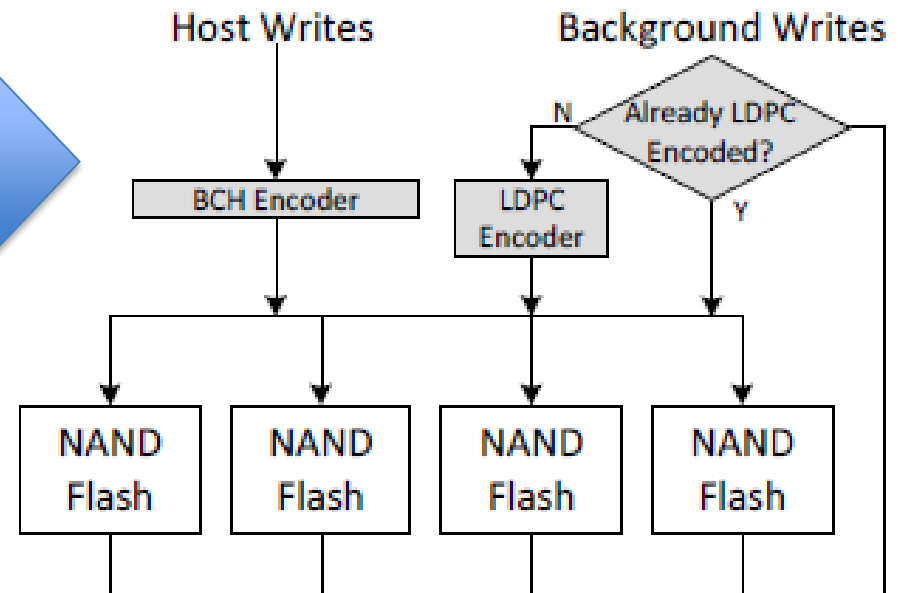
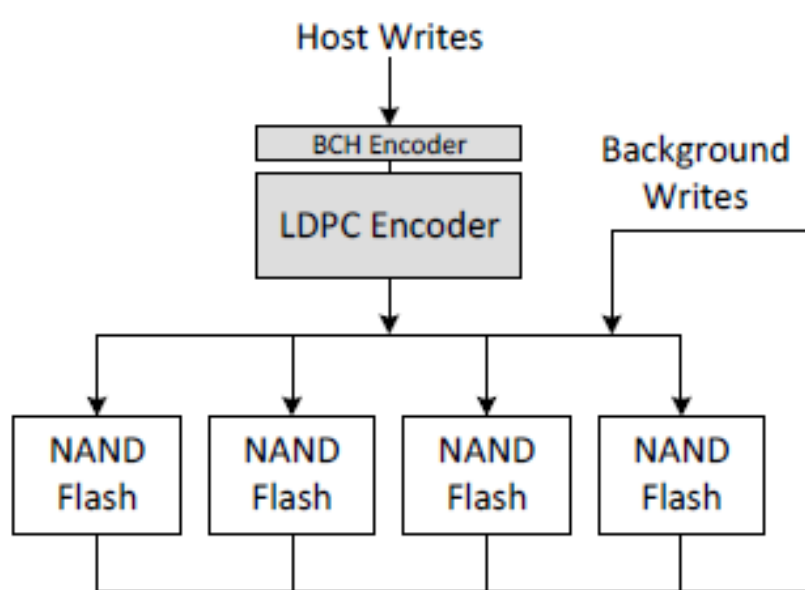
(a) MSRC workloads



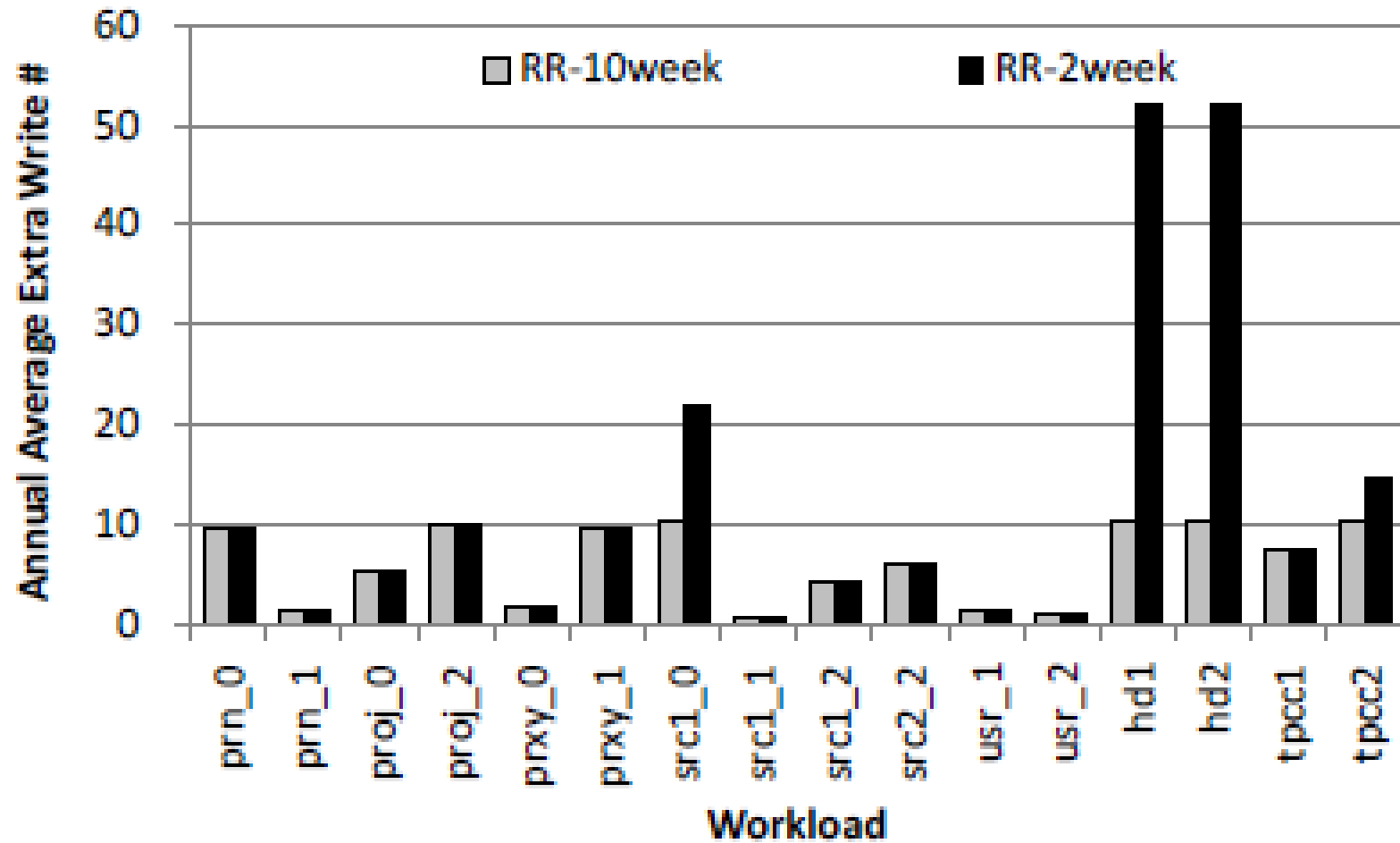
(b) MapReduce and TPC-C workloads

# Retention Time Tracker

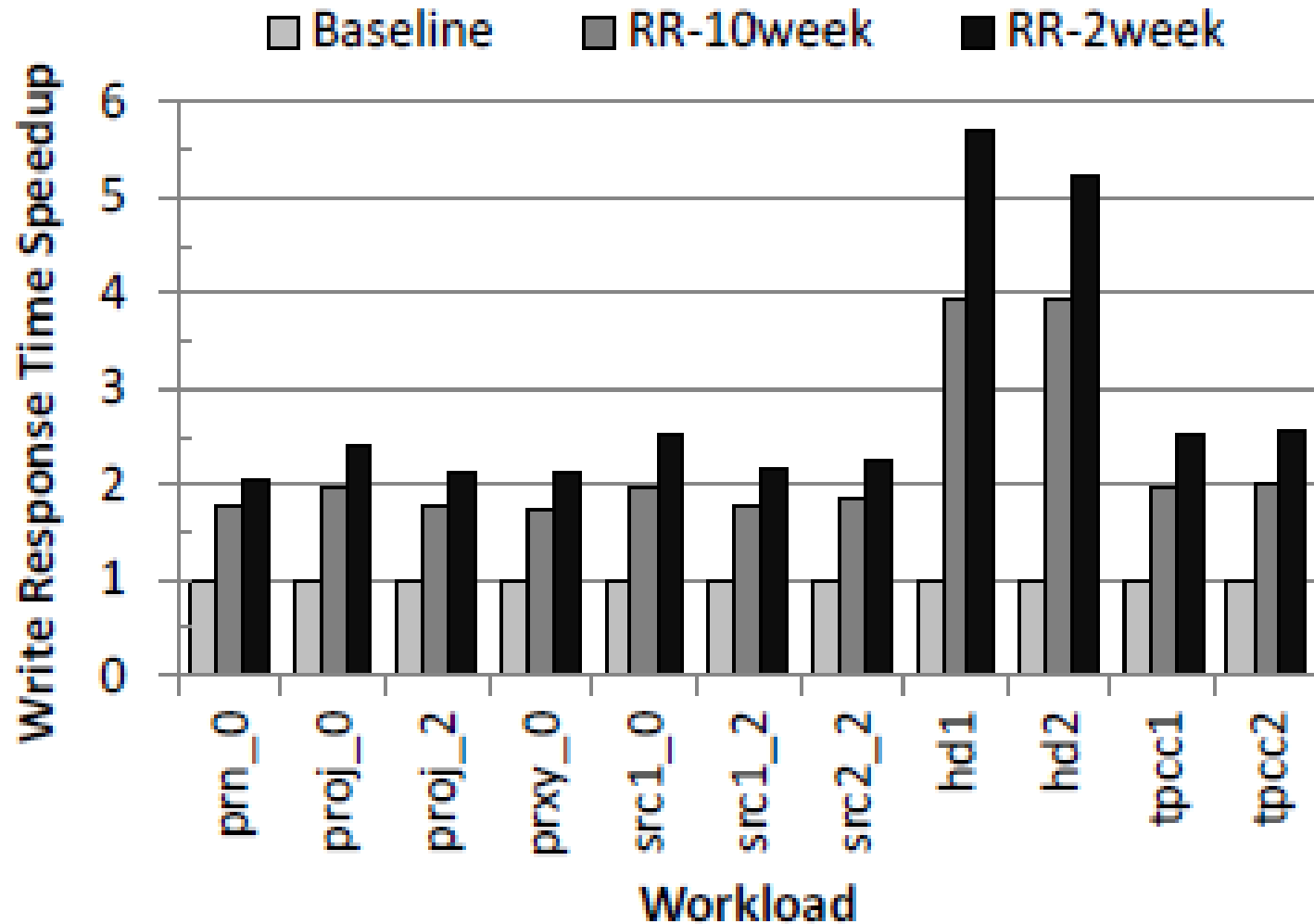




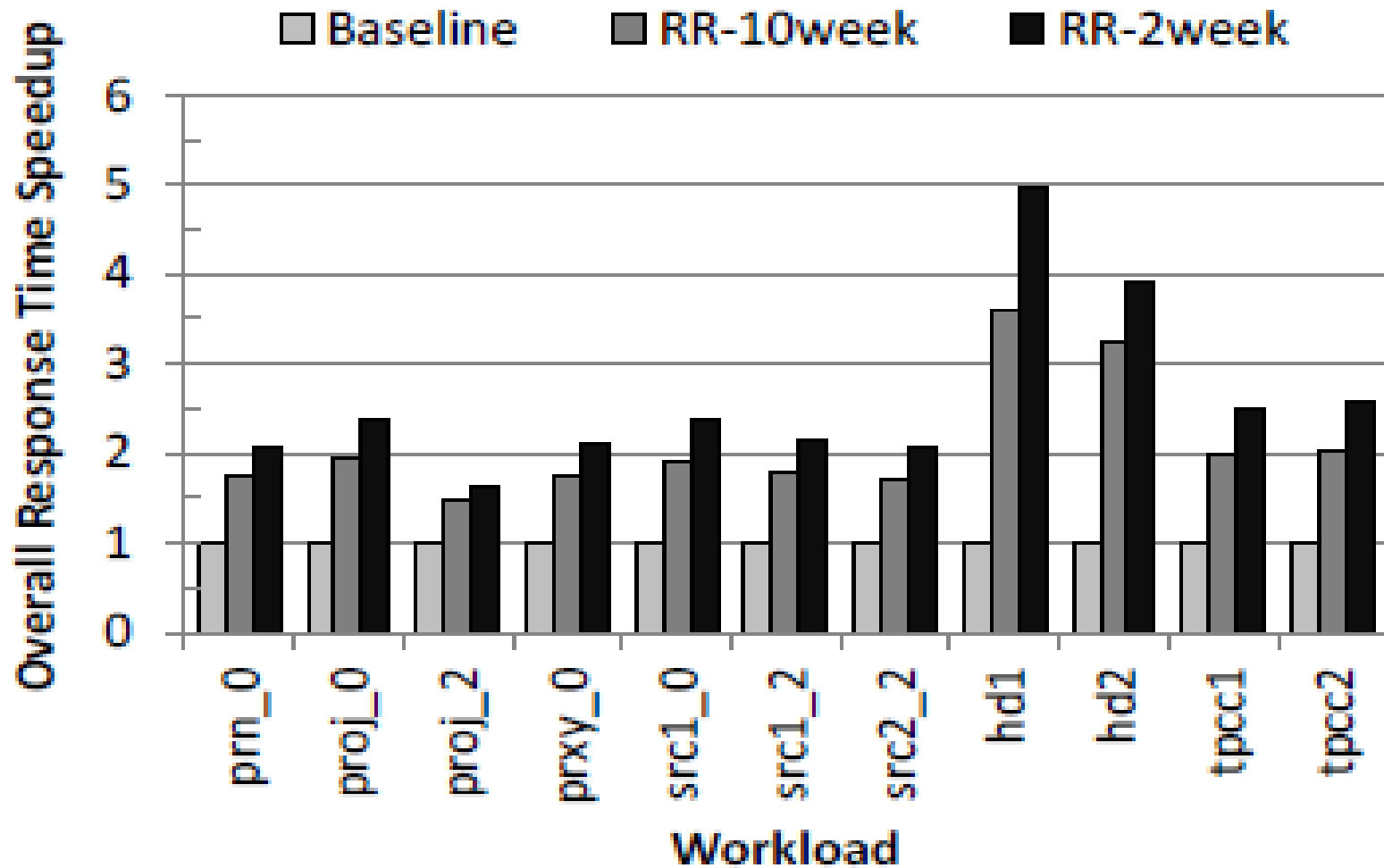
# Extra Write



# Write Speed



# Overall Response Time



They present NAND flash retention relaxation and proposed ECC architecture.

They optimize the write speed and ECC's cost and performance