Practical Nonvolatile Multilevel-Cell Phase Change Memory

Doe Hyun Yoon

Jichuan Chang, Robert S. Schreiber,
Norman P. Jouppi

IBM T. J. Watson
Research Center
PAPER OVERVIEW

- **Issue:**
  - Conventional 4-Level-Cell (4LC) PCM Designs, due to R-drift over time: need refreshes - loose non-volatility.
  - PCM has only finite write endurance
  ~ 10^8 writes per cell
- **Objective:**
  To make MLC-PCM non-volatile with an optimized practical scheme.
- **Proposal:**
  - 3on2 scheme: Observing most errors in 4LC occur in one cell state, use 3-Level-Cell (3LC) PCM to gain non-volatility.
  - Mark&Spare: Low-cost wearout tolerance for 3LC using the unused state in 3LC
- **Result:**
  - Naïve 3LC is genuinely nonvolatile (>10 years retention)
  - Optimal 3LC with Low-cost wearout tolerance, 1.41 bits/cell (vs. 1.52 in 4LC)
    Only 7% lower capacity than (volatile) 4LC
OUTLINE

• PCM, R-drift Background
• Proposal
• Result and Comparison
RESISTANCE DRIFT

PCM Cell resistance increases over time
– \( R(t) \), cell resistance at time \( t \) \((t > 0)\)

A cell is programmed at \( t = 0 \)
Sensed as \( R_0 \) at time \( t_0 \) \((>0)\)

\[
R(t) = R_0 \times \left( \frac{t}{t_0} \right)^\alpha
\]

\( \alpha \): drift rate \((0 < \alpha \leq 1)\)

Drift errors
– Negligible in SLC PCM
– Major reliability problem in MLC PCM
DRIFT ERRORS IN 4LC PCM

4 cell states: S1, S2, S3, S4
– Gaussian distribution

±2.75 σ around mean values

Mean resistance values: μ₁, μ₂, μ₃, μ₄
– Threshold between states: τ₁, τ₂, τ₃

• Drift rate (α) increases with cell resistance
OUTLINE

• PCM, R-drift Background

• Proposal

- 4LC PCM optimal mapping

• Result and Comparison
Drift only increases cell resistance

Optimize $\mu_2$, $\mu_3$, $\tau_1$, $\tau_2$, $\tau_3$ to minimize CER
- minimize $\text{CER}(\mu_2, \mu_3, \tau_1, \tau_2, \tau_3)$
- subject to $\mu_i+2.75\sigma+\delta<\tau_i<\mu_{i+1}-2.75\sigma-\delta$, for $i=1,2,3$

Still need refresh / 17 mins
OUTLINE

• PCM, R-drift Background
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  - 4LC PCM optimized mapping
  - 3LC PCM
• Result and Comparison
3LC PCM

Observation:
– Most errors occur in one state (S3)
DO NOT USE IT
– Wide Margin for S2

Simple and optimal mapping (3LCn & 3LCo)
3LC PCM (3LC$^N$ AND 3LC$^O$)

Reliable for >10 years w/o ECC & refresh
Genuinely nonvolatile
3LC: HOW TO STORE BINARY INFO IN TERNARY CELLS?

3-ON-2
- 9 states in 2 ternary cells
- 8 states for 3-bit data
- 1 INVALID state

Store three bits in two ternary cells
64B (512-bit) data block in 342 cells

INVALID state
- (S4, S4)
- Use this for tolerating wearout failures

<table>
<thead>
<tr>
<th>First cell</th>
<th>Second cell</th>
<th>3-bit data</th>
</tr>
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<tbody>
<tr>
<td>S1</td>
<td>S1</td>
<td>000</td>
</tr>
<tr>
<td>S1</td>
<td>S2</td>
<td>001</td>
</tr>
<tr>
<td>S1</td>
<td>S4</td>
<td>010</td>
</tr>
<tr>
<td>S2</td>
<td>S1</td>
<td>011</td>
</tr>
<tr>
<td>S2</td>
<td>S2</td>
<td>100</td>
</tr>
<tr>
<td>S2</td>
<td>S4</td>
<td>101</td>
</tr>
<tr>
<td>S4</td>
<td>S1</td>
<td>110</td>
</tr>
<tr>
<td>S4</td>
<td>S2</td>
<td>111</td>
</tr>
<tr>
<td>S4</td>
<td>S4</td>
<td>INVALID</td>
</tr>
</tbody>
</table>
OUTLINE

• PCM, R-drift Background
• Proposal
  - 4LC PCM optimized mapping
  - 3LC PCM
  - Mark and Spare: wearout tolerance
• Result and Comparison
TOLERATING WEAROUT FAILURES IN 3LC

PCM has only finite write endurance
– $\sim 10^8$ writes per cell (worse than that for MLC)

Mark-and-spare
– A low-cost wearout failure tolerance for 3LC
– Use 3LC’s INVALID state for marking a cell pair with a failure
– No need to store failed-cell location
– 2 spare cells per failure
MARK-AND-SPARE EXAMPLE

Use INVALID (S4, S4) to mark a cell pair w/ failure

Need a spare pair for tolerating a failure
HOW TO CORRECT WEAROUT FAILURES?
READ DATA PATH
OUTLINE

• PCM, R-drift Background
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  - 3LC PCM
  - Mark and Spare: wearout tolerance
• Result and Comparison
3LCo VS. 4LCo

64B (512-bit) block
• 3LC needs fewer bits than 4LC for error correction
  – 6 wearout failures:
    Mark-and-spare (2 cells/failure) vs. ECP (5 cells/failure)
  – Drift errors: BCH-1 vs. BCH-10
• 3LC: 1.41 bits/cell, 4LC: 1.52 bits/cell
• Besides, 3LC is nonvolatile
SIMULATION RESULT

Simulator configurations

Processor an out-of-order core running at 3.2GHz
L1 cache 16kB instruction and data caches
64B line size
L2 cache 512kB unified cache, 64B line size
MLC-PCM
16GB, 8 banks, 64B blocks
read: 200 ns
write: 1us
write throughput: 40MB/s

Figure 16: Normalized execution time, energy, and power
Other Results and Discussion in the Paper

- Comparison to another paper’s multi-level-cell pcm

<table>
<thead>
<tr>
<th></th>
<th>Data</th>
<th>Wearout failure correction</th>
<th>Drift error correction</th>
<th>Density</th>
</tr>
</thead>
<tbody>
<tr>
<td>4LC in [29]</td>
<td>512 bits / 256 cells</td>
<td>N/A</td>
<td>BCH-32: 320 bits /160cells</td>
<td>1.23 bits /cell</td>
</tr>
<tr>
<td>4LC in our work</td>
<td>512 bits / 256 cells</td>
<td>ECP-6: 31 cells</td>
<td>BCH-10: 100 bits /50 cells</td>
<td>1.52 bits /cell</td>
</tr>
<tr>
<td>3LC in [29]</td>
<td>8 bits / 6 cells</td>
<td>N/A</td>
<td>N/A</td>
<td>1.33 bits /cell</td>
</tr>
<tr>
<td>3LC in our work</td>
<td>512 bits / 342 cells</td>
<td>mark-and-spare: 12 cells</td>
<td>BCH-1: 10 bits /10 cells</td>
<td>1.41 bit s/cell</td>
</tr>
</tbody>
</table>

- Cell Error Rate/Block Error Rate
- Transient Error Correction
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